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RELIABILITY EVALUATION FOR A MULTISTATE DISPLAY AND CONTROL SYSTEM

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Abstract

A multilevel modular decomposition method is employed to analyze and evaluate the reliability of a multistate display and control system. The multistate reliability problem of a system with Built-In-Test (BIT) is handled with this method. It is pointed out that the multistate reliability is corresponding to the concept of quality loss function (QLF) or the deviation from an ideal or target value. The possibility to improve the multistate system reliability with Robust Design methodology is discussed.

Introduction

A basic assumption in most of the reliability literature is that components and the system are binary, i.e., they can only be in either of the two states: perfect (1) or failed (0), and there are no middle states. Thus, the binary models are an oversimplification of the actual reality.

Analyzing avionic system reliability, we often face multistate cases. Most systems degrade over time. Some systems and components may have more than two discrete states owing to their configuration and operating principles. Built-In-Test which has found wide applications in avionics also causes multistate reliability & maintainability situations. Redundancy management and reconfiguration change the states of the system. Moreover, the Variability Reduction Program (VRP), which is a significant aspect in U.S. Air Force's R&M 2000 Process, requires a more accurate quality-reliability evaluation approach to describe the reliability for different states or for different degrees of quality variability of a system. Therefore, we need a powerful and applicable methodology to deal with the reliability problems for multistate avionic systems.

The approaches introduced by most literature concerning multistate system reliability [1-5] are too complex and difficult to be employed in practice because the mathematical complexity and enormous amount of calculation that are needed to compute system reliability. To facilitate the calculation of multistate system reliability analysis, the concept of modular decomposition has been used to decompose large multistate systems and as an aid in developing multistate reliability bounds [6-9]. That represents great progress, but further improvement is needed.

In 1989, Shao and Kapur presented a multilevel modular decomposition approach [10]. It provides a practical approach for engineers and reliability analysts. In this paper, the approach is applied and the following extension and exploration are addressed:

. Analyzing Built-In-Test multistate reliability that is difficult to handle with traditional reliability theory;

. Pointing out that the binary-state reliability is corresponding to the traditional quality control concept of conformance to specification limits, while the multistate reliability is corresponding to the concept of quality loss function or the deviation from an ideal or target value;

. Exploring the approach to improve multistate system reliability with Robust Design methodology.

A case study for a typical multistate display and control system is given to show the multistate system reliability analysis methodology.

Outlines of Multilevel Modular Decomposition Approach for Multistate System

The outlines of multilevel modular decomposition (called multi- decomposition for short thereafter) approach for multistate system [10] are summarized as follows:

. A multistate system is composed of essential components which are configured by a structural function. Let C be the collection of the essential components and Φ be the structure function for the system, the system could be denoted by (C, Φ).

. Every component can be in any of its states $(0, 1, 2, \ldots, M_i$, for $i=1, 2, \ldots, n)$, where n is the number of the components and M_i is the highest state for the i-th component.

. The state set and the state occupancy probabilities of the system depend on the state set and the state occupancy probabilities of the components and the structure function.

. A system can be decomposed to several modules and every module can be decomposed to several submodules, etc.. Hence, there will be several levels for modular decompositions. We can consider a modular decomposition as an operating procedure or an organizing action and a module as a substance. The objects with which a certain level modular decomposition deals are one-level-lower submodules and the product it yields is a new and same level module. The multilevel modular decomposition method does not change the state set and the state occupancy probabilities of the system but greatly reduces the amount of calculation.

- For every decomposition, there is a corresponding structure function. In the state tree, every gate (denoted by G_j^k) is actually a decomposition and a structure. The easiest to understand structure function is the tabular function.
- The state tree is used to graphically indicate the logical relationship among the states of components, subsystems and the multistate system. All the standard symbols in the fault tree analysis (FTA) except the AND and the OR gate are used to construct a state tree and describe the states of events and their logical connections. Both AND and OR gates are replaced by a STATE gate along with the event state values.
- The occupancy probabilities of the J-th equivalence class of the k-th level, j-th module is

$$P_{Jj}^{k}=P_r\,[G_j^k(X_j^k)=J]=P_r\,(X_j^k\in S_{Jj}^{k}) \qquad (1)$$

and the corresponding reliability is

$$R_{Jj}^{k}=P_r\,[G_j^k(X_j^k)\geq J]=\sum_{i=J}^{M_j^k} Pr\,[G_{Jj}^{k}(X_{Jj}^{k})=i] \qquad (2)$$

where $k=0, 1, \ldots, L$; $j=1, 2, \ldots, u_k$, and X_j^k is the state vector of the k-th level, j-th module, S_{Jj}^{k} is the state vector space for the J-th equivalence class for the module and $G_j^k(X_j^k)$ is the structure function for the module which is the random variable giving the state of the module $(C_j^k,\ G_j^k)$.

- The Performance function of module (C_j^k, G_j^k) is denoted by h_j^k. It is defined as follows:

$$h_j^k=\sum_{J=0}^{M_j^k} J\cdot P_{Jj}^{k} \qquad (3)$$

When k=1, j will be a unity. Then $R_J=R_{1J}^{L}$ is denoted as the J-th state reliability of the multistate system and $h=h_1^L$ as the performance measure of the multistate system.

Reliability Analysis of a Multistate Display and Control System

A hypothetical display and control system is used as an example of the multistate system to describe the methodology presented in this paper.

Block Diagram for the System

The hypothetical airborne display and control system in Figure 1. consists of a BIT and the following nine components (LRUs): DCMP-1 (Displays and Controls Management Processor), DCMP-2, UFCP (Up Front Control Panel), AAP (Avionic Activation Panel), MFD-1 (Multi-function Display), MFD-2, MFCD(Multi -function Color Display) , VTR (Video Tape Recorder) and VCP (VTR Control Panel).

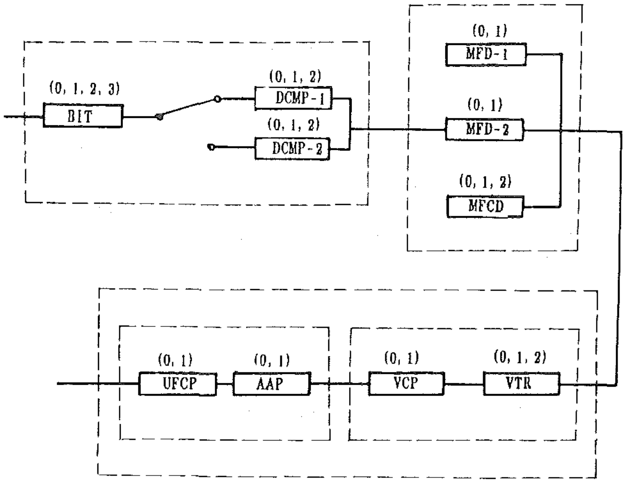

Figure 1. Block Diagram for the Multistate Display and Control System

In the hypothetical system, the two DCMPs form a warm standby subsystem. The display subsystem consisting of two MFDs and one MFCD is a 2-out-of-3:G one.

In avionics systems, the Built-In-Test (BIT) technology has been widely used. But it is difficult or even impossible to analyze its reliability precisely with the traditional binary reliability theory, for the BIT is usually of multi-state. With the methodology presented in this paper, the BIT reliability analysis can be implemented satisfactorily. The BIT in this example is used to monitor and test all the LRUs and control the switching of the warm standby subsystem which is composed of two DCMPs. To facilitate the logic, suppose that the redundancy management of the 2-out-of-3:G display subsystem is performed by the pilot rather than BIT. Hence, except the warm standby DCMP subsystem, BIT does not affect the function of the other LRUs. Therefore, the BIT is considered to be a part of a module consisting of 2 DCMPs and the BIT.

By the way, it is also possible to consider that the 2-out-of-3:G display subsystem is controlled by BIT. In that case, we may assign a second BIT to construct a composition together with the 2-out-of-3:G subsystem. However, the reliabiity model will become more complicated.

Suppose that UFCP, AAP, MFD-1, MFD- 2 and VCP have two states respectively: 0 (failed) and 1 (perfect). While DCMP-1, DCMP-2 and MFCD have three states each: 0 (failed), 1 (OK) and 2 (perfect), and BIT has four states:

0(failed), 1(fault undetected), 2(false alarm) and 3 (perfect).

The symbols used in the reliability block diagram for the binary system can be used in Figure 1. , but their definitions have been extended. Every rectangle (▭) along with the state values marked above depicts a multistate component.

Multistate Tree of the Display and Control System

It is possible to describe multi-decomposition of the multistate system in a reliability block diagram (see the dotted-line rectangles in Figure 1.), but the detailed information has not been indicated. With a multistate tree, there will be no problem to graphically and clearly depict all the information on multi-decomposition of the hypothetical Display and Control System (see Figure 2.).

Components State Occupancy Probabilities

The probabilities of every component being in various states or state occupancy probabilities are given in Table 1.

Reliability Calculation

There are many methods to depict a structure function such as the tabular function, value vector, or lattice expression[11] . In this paper, the approach of tabular function is adopted for its easy understanding. However, the analytical structure functions are more suitable for computer-aided reliability analysis. The following Tables 2.1-2.6 indicate the structure function for each decomposition $G_j^k(X_j^k)$:

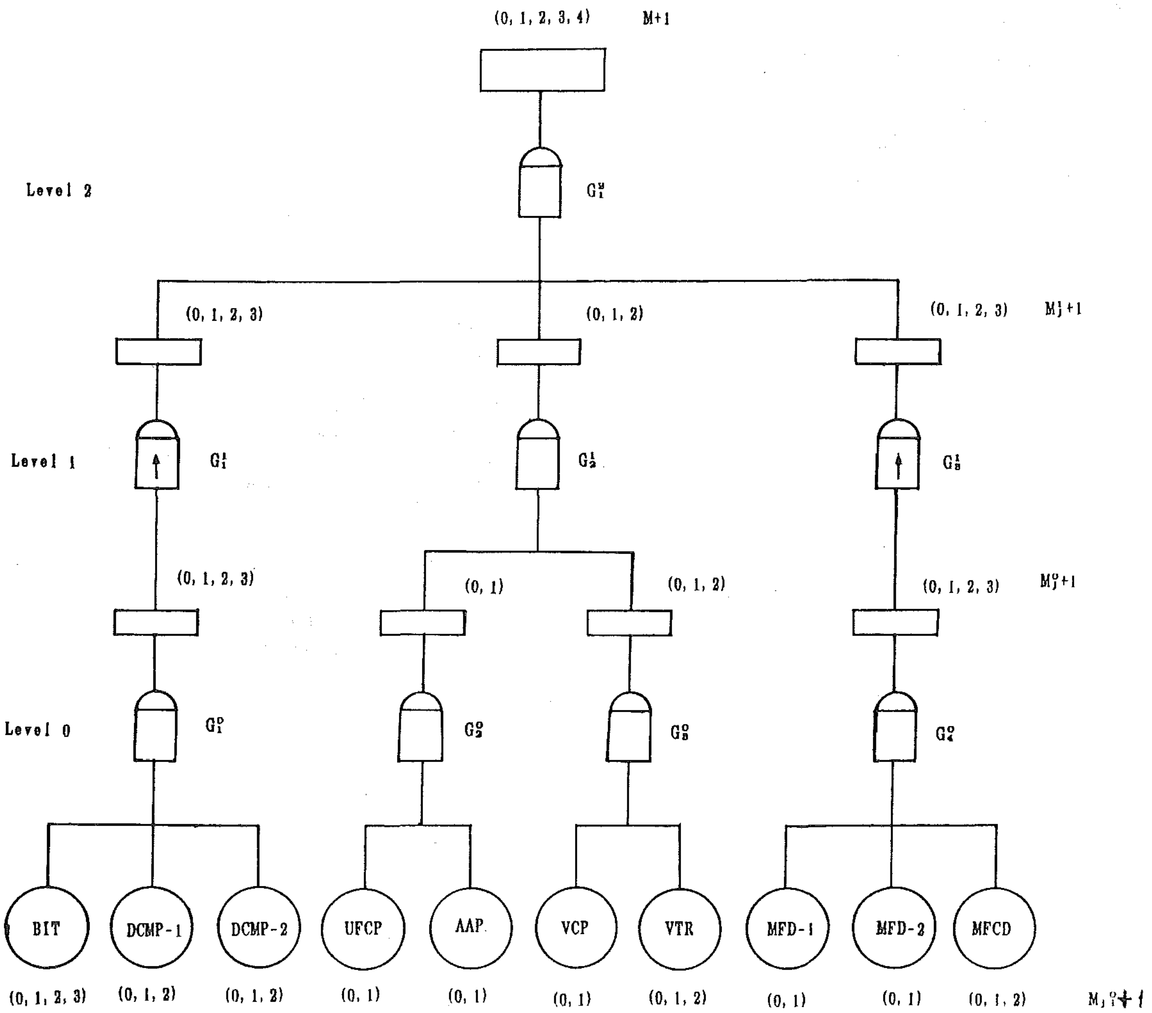

Figure 2. State Tree for the Display and Control System

Table 1 Component State Occupancy Probabilities

State	0	1	2	3
BIT	0.005	0.01	0.10	0.885
DCMP-1	0.01	0.19	0.8	
DCMP-2	0.01	0.19	0.8	
UFCP	0.05	0.95		
AAP	0.01	0.99		
VCP	0.05	0.95		
VTR	0.02	0.10	0.88	
MFD-1	0.05	0.95		
MFD-2	0.05	0.95		
MFCD	0.05	0.15	0.80	

Table 2.1

G_1^0	No. of State Vectors	{BIT, DCMP-1 DCMP-2 }	P_{1j}^0	R_{1j}^0
0	16	All of the state vectors with the BIT in state (0) and 100, 200, 300, 101, 102, 210, 220	.0062	
1	9	301, 310, 311, 110, 112, 201, 211, 221	.0566	.9935
2	6	202, 212, 222, 302, 320, 120	.0942	.9376
3	5	322, 321, 312, 121, 122	.8434	.8434

$h_1^0=2.7752$

Note: When BIT is in state 3(perfect), DCMP-1 in state 0 (failed) or 1 (OK), and DCMP-2 in state 2(perfect), the DCMP-2 will work as the main unit. At this point, if DCMP-1 is in state 1 (OK), it will work as the standby unit. The reasons to determine the states of the module shown in Table 2.1 will be explained in detail in the Section "Multistate Reliability of BIT" later on.

Table 2.2

G_2^0	No. of State Vectors	{ UFCP, AAP }	P_{2j}^0	R_{2j}^0
0	3	00, 01 10	.0595	
1	1	11	.9405	.9405

$h_2^0=0.9405$

Table 2.3

G_3^0	No. of State Vectors	{ VCP, VTR }	P_{3j}^0	R_{3j}^0
0	4	00, 01, 02, 10	.0690	
1	1	11	.0950	.9310
2	1	12	.8360	.8360

$h_3^0=1.7670$

Table 2.4

G_4^0	No. of State Vectors	{ MFD-1, MFD-2 , MFCD }	P_{4j}^0	R_{4j}^0
0	5	000, 001, 010, 100, 002	.0073	
1	5	011, 012, 101, 102, 110	.1353	.9927
2	1	111	.1354	.8574
3	1	112	.7220	.7220

$h_4^0=2.5721$

Note: When any one of three multi-displays fails, the pilot will reset the other two ones with the multi-displays' On/Off controls to perform all the display and control functions.

$G_1^1=\{G_1^0\}$, $h_1^1=h_1^0=2.7752$

Table 2.5

G_2^1	No. of State Vectors	{ G_2^0, G_3^0 }	P_{2j}^1	R_{2j}^1
0	4	00, 01, 02, 10	.1244	
1	1	11	.0893	.8756
2	1	12	.7863	.7863

$h_2^1=1.6619$

$G_3^1=\{G_4^0\}$, $h_3^1=h_4^0=2.5721$

Table 2.6

G_1^2	No. of State Vectors	{ G_1^1, G_2^1, G_3^1}	P_{1J}^2	R_{1J}^2
0	30	All of the state vectors with at least one 0	.1898	
1	14	All of the remained state vectors with at least one 1	.1391	.8102
2	1	222	.0100	.6711
3	2	322, 223	.1823	.6611
4	1	323	.4788	.4788

$R_1=0.8102$, $R_2=0.6711$
$R_3=0.6611$, $R_4=0.4788$
and $h=h_1^2=2.6212$

Cumulative Efficiency Index (CI)

Using Equation (10) given by Reference [10] and substituting the data shown in Figure 2., the Cumulative Efficiency Index is obtained as follows:

$$CI=0.0123$$

This shows that the amount of reliability calculation using this method is 1.23% of that using the traditional one.

Multistate Reliability of BIT

Built-In-Test (BIT) technology has found wide applications in sophisticated system, such as aeronautical and astronautical ones. The BIT system is a very capable and powerful equipment: it can not only detect system failures, but also distinguish and report the failure mode and the occurrence time, and isolate the fault to a certain LRU, and record all the information.

In order to apply BIT technology and/or analyze BIT systems, one must be aware of the parameters of BIT and take them into account of the system reliability analysis.

When BIT does not influence the operation of the system in its reliability, it can be considered as a test unit in a series system which consists of the original system and BIT.

But if BIT plays a role in redundancy management and reconfiguration of the system, it does affect the system operation, and the situation becomes very complicated. For a redundant system with BIT, if BIT can not detect a failed active unit, the system may fail. And moreover, BIT has a certain false alarm rate that causes a rejection of a normally working unit and disconnects it from the system.

From the above description, it is very clear that it is difficult or even impossible to carry out the BIT reliability analysis of the redundant system with BIT by the traditional reliability theory, in which the components are binary.

The work done in this paper shows that the multistate reliability methodology can be applied to BIT reliability analysis, and the result is satisfactory.

Now consider the situation that BIT tests and monitors DCMPs in the above example. In the system, BIT takes part in the redundancy management.

Suppose that BIT has four working states in the system, which are 0 (failed), 1 (fault undetected), 2 (false alarm) and 3 (perfect). If BIT itself fails, the series system composed of BIT and the original system can not work, and BIT is considered to be in state 0 (failed). When BIT works but can not detect whether the active unit fails and the system redundancy can be controlled, BIT is considered to be in state 1 (fault undetected) and the system state is determined by the state of the active unit. If BIT works, but issues a false alarm, the state of the system is determined by the state of the standby component and BIT is considered to be in state 2 (false alarm). When BIT works perfectly, it is called to be in state 3 (perfect).

In the example of this paper, BIT tests and monitors DCMP-1 and DCMP-2, and takes part in the system redundancy management. With the multistate reliability analysis of BIT, the system reliability can be evaluated accurately (see Table 2.1).

Improve System Reliability with Robust Design [12]

For many cases, product reliability can be viewed as the probability that the function variation is less than its critical failure value, and so the product will perform the required functions under stated conditions for a stated period of time. In the view of quality, product reliability is actually quality characteristic of duration of the product.

Therefore, reliability can be improved with variation reduction methodology. Robust Design, which is a modern and advanced set of approaches to design quality and reliability into the products, includes QFD, Taguchi's Method, Design of Experiments (DOE), SPC, and etc.. The following section explores the approach to improve multistate system with Robust Design.

QLF and Multistate Reliability

The traditional quality evaluation method is to inspect whether the quality characteristics of a product conform to specifications. That means the product is either qualified (conforming to specifications) or not qualified (not conforming to specifications). Corresponding to that, the traditional reliability evaluation method distinguishes the system or components into two states: i.e., either in function (1) or in failure (0). When the system or components are within the critical failure limits, they are functioning. Otherwise, they are failed.

The traditional quality and reliability assessment criterions are illustrated in Figure 3., where f(x, t) is the probability density function (pdf) of the product quality characteristic (random variable) X and time t. The mathematical expectation, the variance and the design target of X are denoted by μ, σ and m respectively. The upper and lower limits of tolerance are denoted by S_u and S_l, and the upper and lower critical failure limits are denoted by T_u and T_l.

When the quality characteristic is within T_u and T_l, the item is functioning (1) equally. Otherwise, they are failed (0) equally. However, For many quality characteristics, the difference in reliability for an item just within the lower and upper critical failure limits from the one just outside may be slight, but one is considered to be "functioning" and the other one is considered to be "failed". From the above analysis, the traditional binary reliability model is not fit for the practical situation.

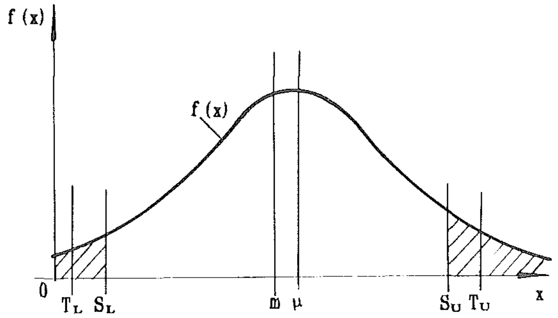

Figure 3. The Traditional Quality and Reliability Assessment Criterions

In the late 1970s, Dr. Genichi Taguchi presented the concept of quality loss function (QLF), which is used to establish the relationship between quality loss and the variability of product quality characteristic (or the variation of quality characteristic from the target value).

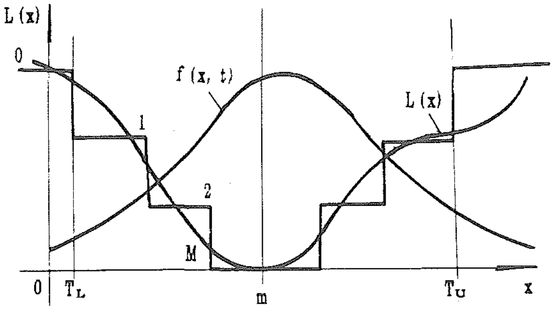

Figure 4. QLF and the Multistate Reliability

For reliability analysis, QLF can be used to define the states for reliability of the system or components. The less the quality characteristic deviates from the target value m, the more reliable the system or components are. We may describe the fact with discrete reliability levels as shown in Figure 4.. Obviously, the quality loss caused by the product that only can perform the basic function is larger than that caused by the product that performs perfectly. Thus, the product multiple state in reliability analysis can be determined by its QLF in the discrete form. The highest reliability level (M) represents the least quality loss, while the lowest level (0) represents the failed state which causes large quality loss.

Improve Product Reliability with Robust Design

In Figure 4., f(x, t) is the quality characteristic pdf of a batch of products (assume it is normally distributed). At time t, the mean of the pdf, the standard deviation and the mathematical expectation of quality loss of this batch are denoted by μ, σ and L respectively. Then

$$L = \int_X L(x)\, f(x, t)\, dx \approx k[\sigma^2 + (\mu - m)^2] \qquad (4)$$

where L, μ, σ are all the functions of time t.

It has been pointed out in the last section that the multistates of a product in reliability are corresponding to the discrete form of QLF. The higher the state of the product, the less the quality loss L. Then, in order to improve the reliability, we should reduce quality loss as much as possible.

There are two ways to reduce the quality loss of a product:

- Minimize the product function variation, i.e., minimize $[\sigma^2 + (\mu - m)^2]$, in order to improve the shape and the location of the quality characteristic pdf.
- Minimize the quality loss factor k in order to make the quality loss curve flatter.

Moreover, Robust Design employs Quality

Function Deployment (QFD) method to determine the critical characteristics and aspects for design, process and manufacturing. Then the

parameter design and tolerance design are employed to enable products insensitive and resistant to the environment, component degradation and aging, manufacturing variations, etc..

In a word, Robust Design will improve the reliability of products essentially.

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