SIC INVERTER OPTIMIZATION FOR HIGH TEMPERATURE APPLICATIONS

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Abstract

SiC devices enable high temperature operation of power converters. The paper analyzes the operation of a high temperature inverter demonstrator, the operation at the device level, the interaction with respect to gate drivers and the possible optimization. Demonstrators were achieved in the framework of the SEFORA project. SiC-JFET devices were obtained from SiCED. A full inverter has been packaged in a Si3N4 module.

1 Introduction

A 3-phase inverter is a suitable pilot converter to demonstrate high-temperature operation up to 200°C. Different studies have shown the feasibility of inverters working at such temperatures using SiC JFETs as power switches. Different high temperature applications are concerned with the proposed study. Aircraft applications are for example SMART-EMA (Electro Mechanical Actuator) for braking systems (1 to 5 kW) and for engine speed control (1 to 2 kW). The specific mission profile is briefly described. The research program SEFORA focuses on the prototyping of a 3-phase JFET voltage inverter including adapted and reliable packaging for high temperature applications, gate drivers, high-temperature capacitors, high-temperature voltage, current and temperature sensors and protection schemes. A pilot converter is designed with the following specifications:

- supply DC bus: 540V
- output current : 6 A per leg output
- switching frequency: 10 kHz to 30 kHz
- JFET junction temperature: up to 250 °C
- package ambient temperature: -55 °C to 200 °C.

To avoid reliability problem with SiC schottky diodes, a diode-less inverter structure has been selected.

2 JFET characterizations

2.1 *Degradation characteristics of a SiC-JFET*

Since some studies have shown that a degradation phenomena occurs in high voltage SiC MOSFETs [1]. We have investigated such phenomena on SiC-JFETs. So, a severe condition test was planned by applying a constant reverse current which corresponds to the maximum line current, flowing in the internal diode of the JFET during the freewheeling. In this worst case the degradation should be maximal with respect to the normal

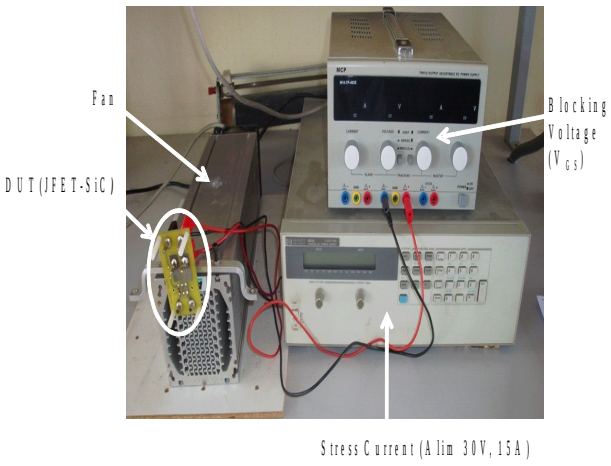

Fig. 1: *test bench for measuring the degradation of a JFET*

operation where the freewheeling phase only occurs durring the inverter dead-time, i.e. from 500 ns to 1 µs. The measurements should therefore consider the possible evolution of some electrical characteristics like the on-resistance, and the saturation current as a function of time.

Description of the workbenches

Fig. 1 and Fig. 2 shows the test bench and the associated circuit for measuring the degradation of a JFET.

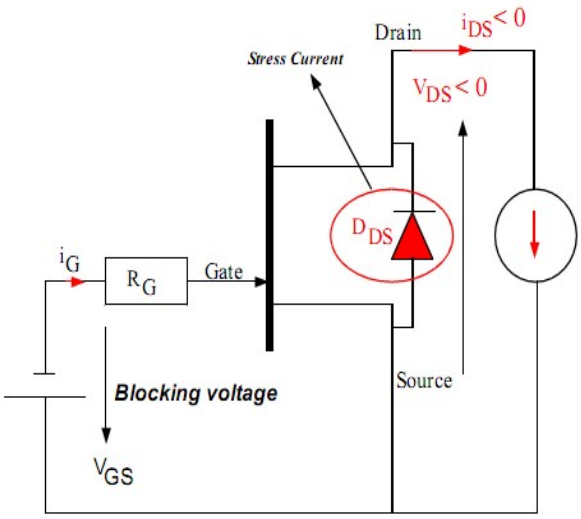

Fig. 2: Principle circuit *for measuring the degradation of a JFET*

The circuit includes two power supplies, the first one to block the JFET and the second one to apply the permanent stress. The measurement process is the following:

- Blocking the JFET by applying a negative voltage on its gate (blocking voltage)
- Applying a permanent stress with a reverse current in the JFET under test.
- Measuring the electrical characteristics of the JFET during the stress at different sampled times by interrupting the stress during the measurements.

Degradation results

Fig. 3 and Fig. 4 represent the results of a degradation of a SiCED-VJFET 1200V(Set 02 INF04 n°69, 2.4 x 2.4 mm²) for a stress current of I=5A. That shows the evolution of the on-resistance and the saturation current for a stress current of 64h. There are a small increase (7%) of the R_{ON} and this resistance reaches a limit at t = 34 h. So, a degradation process may exist but it is completely different form the degradation process described in [1]. The impact is very weak and remains fully acceptable for industrial applications. The same degradation protocol was applied to 8 A and 10 A, yielding to similar results.

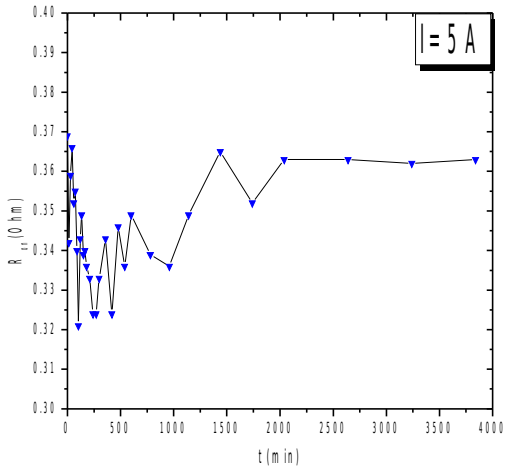

Fig. 3: *Degradation of the on-resistance during a 64h stress with a 5 A reverse continuous current for a SiC-JFET form SiCED (2.4 x 2.4 mm²).*

Since the applied stress constraints were very strong, those results validates the diode-less inverter structure particularly for high temperature applications.

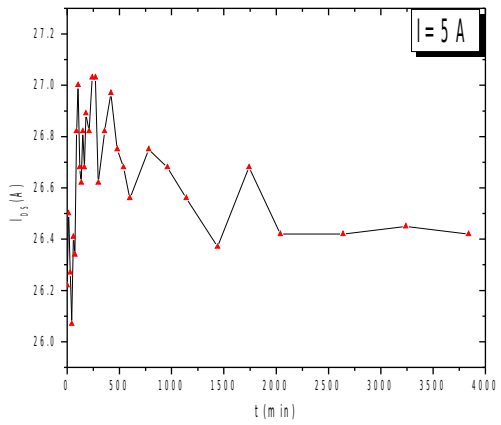

Fig. 4: *Degradation of the saturation current during a 64 h stress with a 5 A reverse continuous current for a SiC-JFET form SiCED (2.4 x 2.4 mm²).*

2.2 Electrical Characterization of JFETS.

The electrical characteristics of the JFET devices used in our prototype are dies having an area of 2.4 x 2.4 mm². They were characterized in [2]. Here characterization on new dies having an area of 4.16 x 4.16 mm² are presented.

Steady state characteristics in forward bias of a SiCED/INFINEON JFET.

To characterize a SiC JFET transistor at steady state, a positive bias between drain and source is applied, while the gate voltage is decreased from 0 down to the pinch off voltage. A curve tracer, Tektronix 371A, was used for these characterizations. Fig. 5 and Fig. 6 shows the steady state electrical characteristics in forward mode at 25 °C and 300 °C respectively.

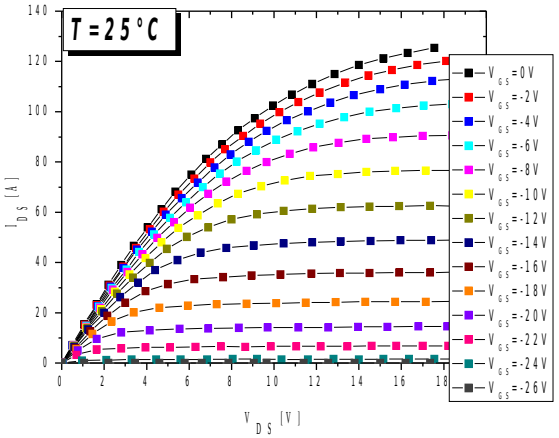

Fig. 5: *Steady state characteristics in forward bias mode of the SiCED-JFET lot HY064 at room temperature (left) and at 300°C (right)*

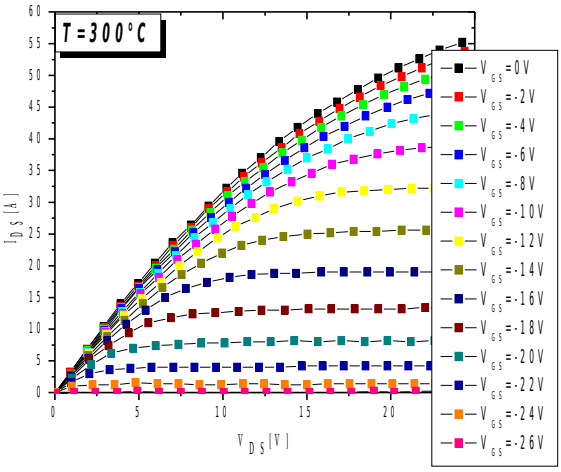

Fig. 6: *Steady state characteristics in forward bias mode of the SiCED-JFET lot HY064 at room temperature (left) and at 300°C (right)*

Fig. 7 and Fig. 8 show the variation of the on-resistance, R_{ON} , and the saturation current I_{DS}^{SAT} , versus temperature respectively. It can be observed the increase of the on-resistance and decrease of the saturation current with increasing temperature. This phenomenon is due to the decrease of the carrier mobility for increasing temperature.

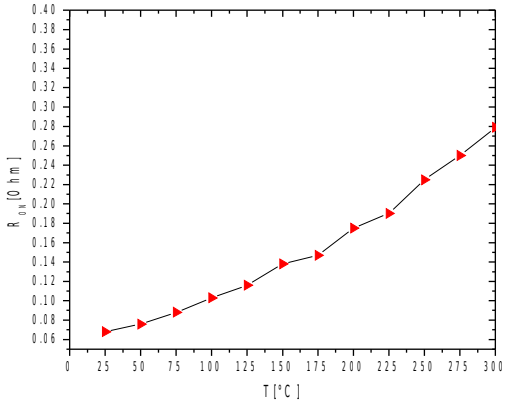

Fig. 7: O*n-resistance,* R_{ON} *, versus temperature for a SiCED JFET in lot n°HY064 (4.16 x 4.16 mm²).*

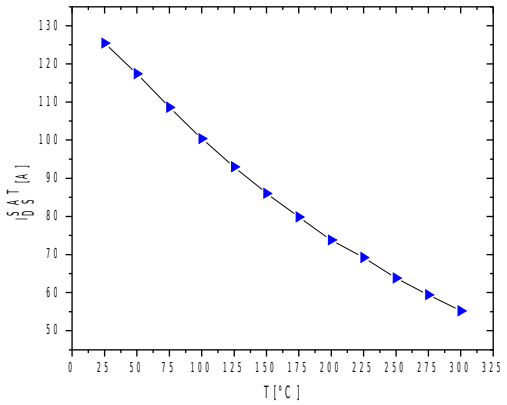

Fig. 8: S*aturation current ,* I_{DS}^{SAT} *, versus temperature for a SiCED JFET in lot n°HY064 (4.16 x 4.16 mm²).*

Gate-source Characteristics

Fig. 8 and Fig. 9 show the current-voltage characteristics of the gate junction in forward and in reverse biases, respectively. The characteristics are obtained with a tracer, Tektronix 370A.

Fig. 8 is typical from a wide band gap semiconductor because of the high threshold,

about 2.5 V, instead of about 1 V in silicon devices.

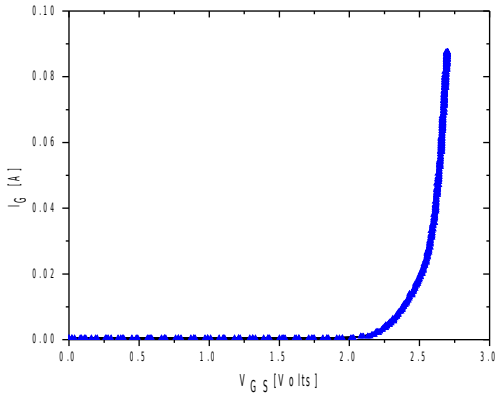

Fig. 9: *Current-voltage characteristics of the gate junction in forward mode for a SiCED-JFET (4.1 x4.1 mm²) in lot n°HY064*

Fig. 9 is typical from a punch-through phenomena because of the soft break instead of a strong break in case of an avalanche breakdown. The punch-through current is a current flowing between the two P+ regions through a depleted N region (Fig. 11). The hole carriers have a barrier height to pass through.

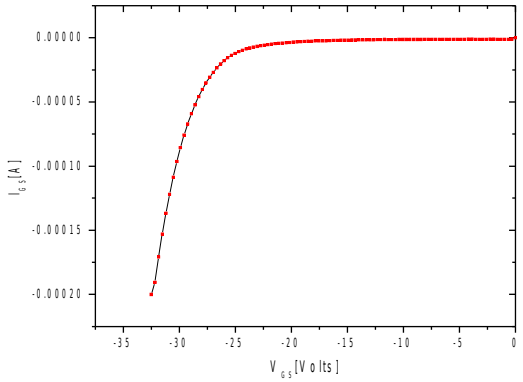

Fig. 10: *Current-voltage characteristics of the gate junction in reverse mode for a SiCED-JFET (4.1 x4.1 mm²) in lot n°HY064*

2 Driver

A JFET is a normally-on power switch which requires a negative voltage across the Gate-Source pins to be in an Off-state. Two specific values have to be considered to block the JFET in static and dynamic mode as described in this section, the threshold voltage V_{T0} and the breakdown Gate-Source voltage $V_{br,gs}$ (or punch-through voltage). Besides, different driving strategies are presented to manage with V_{T0} and $V_{br,gs}$.

The results presented in this section were performed with 4H-SiC power Vertical JFETs (1200V, 0.4Ω) from SiCED. Fig. 11 illustrates the schematic cross section of a half cell for VJFET which is detailed in [3], and a corresponding equivalent electrical circuit which takes into account its static and dynamic behaviours.

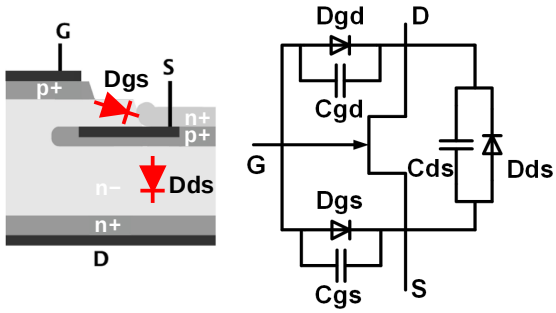

Fig. 11: SiC VJFET cross section and equivalent circuit.

3.1 SiC JFET Gate behaviour

3.1.1 Static behaviour

To turn off a JFET, the internal gate-source diode *Dgs* (Fig. 11) has to be reverse biased. As mentioned in a previous section of this paper and in other papers [3-5], when a negative and a significant voltage is applied to block *Dgs*

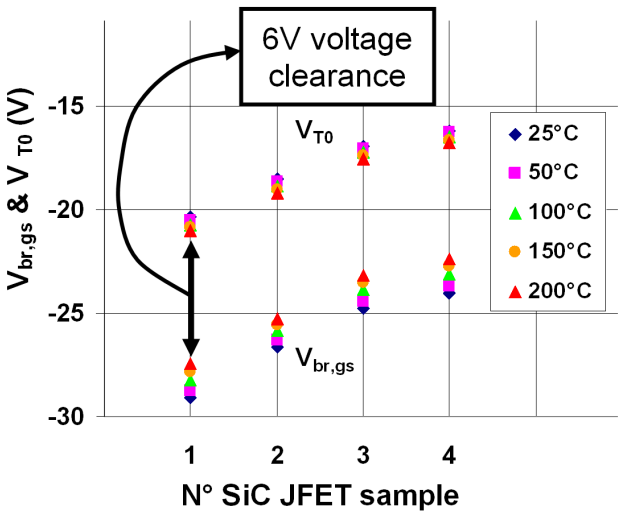

Fig. 12: Behavior of SiC JFET gates on 4 samples at temperatures up to 200°C. Top : Threshold gate-source voltage VT0 - Bottom : Breakdown gate-source voltage Vbr,gs

(slightly below V_{T0} and greater than or equal to $V_{br,gs}$), a gate current appears due to the punch-through effect.

Fig. 22 shows a gate characterization in reverse bias of 4 JFET samples at temperatures from 25°C to 200°C. Threshold gate-source voltage V_{T0} and breakdown gate-source voltage $V_{br,gs}$ are measured. V_{T0} remains almost constant while $V_{br,gs}$ slightly diminishes at 200°C, leaving a voltage clearance of 6 V between V_{T0} and $V_{br,gs}$. So, the blocking voltage has to be chosen in keeping in mind the two specific values, V_{T0} and $V_{br,gs}$.

3.1.2 Dynamic behaviour

In this part, a study of one JFET leg (Fig. 14) of a voltage source inverter is presented to show drain-to-gate interaction impacts. Fig. 13 depicts the switching curves of the JFET working in free wheeling mode (J_H) to highlight gate-source voltage disturbances during the dead time. Indeed, during turn-on or turn-off of the internal drain-source diode of J_H, the driver cannot apply correctly the negative gate bias because of a significant gate impedance (R_G, l_G). Thus, the JFET low gate-source capacitance *Cgs* cannot act as a sufficient decoupling capacitor. This is why, because of the gate-drain capacitance Cgd, a negative spike appears on V_{gs_H} due to the variations of drain-source voltage during turn-on, which can conduct to the punch-through issue of the gate-source junction during. This may damage the JFET gate by thermal effect.
On the other hand, at turn-off, a positive peak appears on V_{gs_H}, which can lead to the short-circuit of the inverter leg.
To minimize these undesired effects for the JFET legs and consequently for the SiC JFET inverter, several SiC JFET gate driver circuits are presented, see part 3.2.

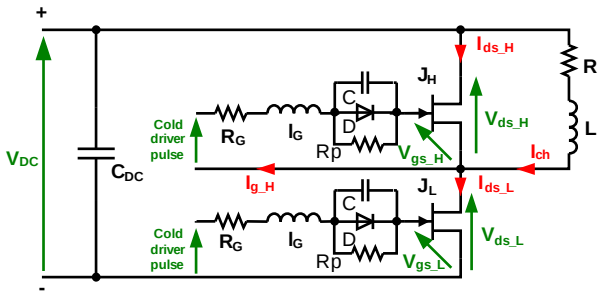

Fig. 14: Setup used to show drain-to-gate interaction

However, a simple way to reduce considerably drain-to-gate interaction impacts consist in decreasing the gate impedance (R_G, l_G) especially l_G, which is detailed in [5].

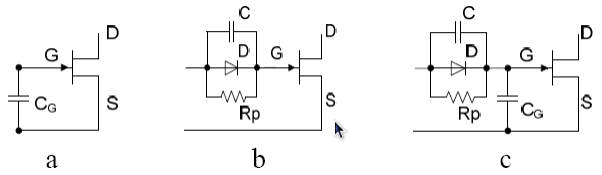

Fig. 15: Three specific SiC JFET Gate Driver Circuits

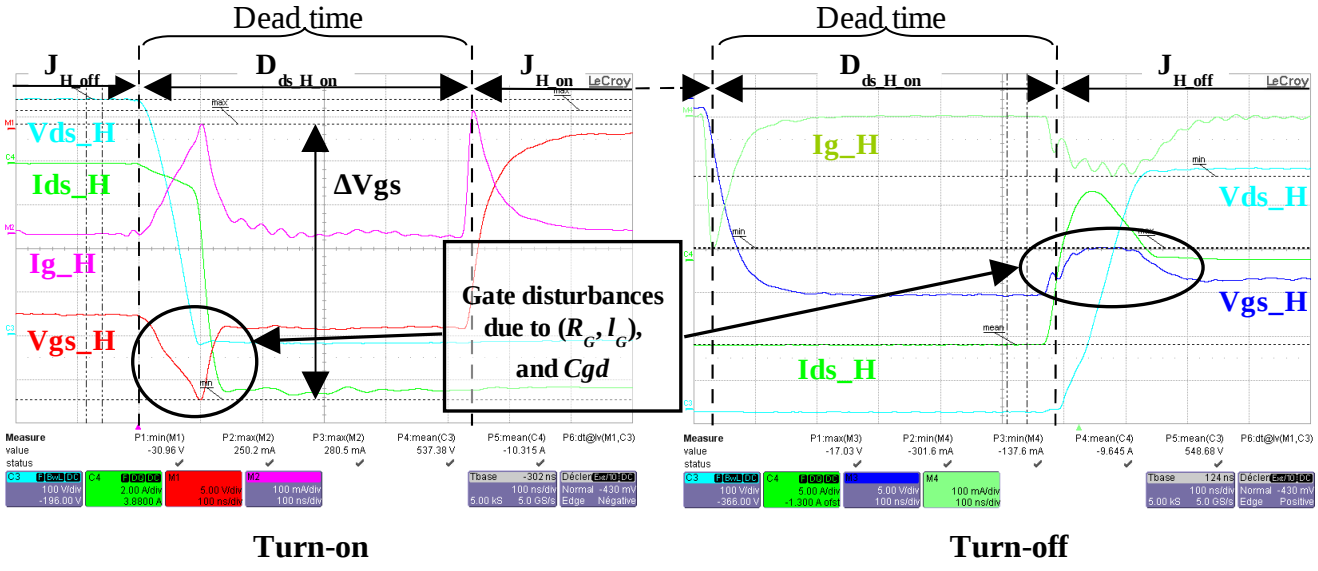

Fig. 13: Switching curves of JFET J_H working in free wheeling mode 540V on DC bus voltage, 10A switched current. V_{T0} = -19.2V, Blocking voltage = V_{T0}-3V, T =25°C. During J_H turn-on, its gate operates in punch-through condition since ΔVgs□-31V<Vbr,gs.

3.2 SiC JFET Gate Driver Circuits

To turn-on or turn-off a SiC JFET, a specific gate driver circuit is required to avoid damaging the JFET gate or the inverter due to drain-to gate interaction effects mentioned in part 3.1. We present in this paper three specific gate driver circuits:

- The first one proposed in [5] consists of an external capacitor C_G connected between Gate-Source pins (Fig. 15-a). C_G acts as a decoupling capacitor to minimise gate-to-drain interaction effects. The advantage of this solution is to insure a protection against the punch-through issue of the JFET Gate, both in static and dynamic mode. However, the blocking voltage has to be tuned below V_{T0} and above $V_{br,gs}$, and the right choice of the C_G value depends on the blocking voltage, $V_{br,gs}$, the gate impedance (R_G, l_G), the DC bus voltage, the converter efficiency (inverter+driver) and the ambient temperature.

- The second one proposed in [6] is composed of a parallel circuit (R_p // C // D) placed in series with the JFET gate (Fig. 15-b). C has to be well dimensioned to block the JFET; usually the minimum value of C is equal to ten times the value of the equivalent capacitance of JFET between Gate-Source pins. At JFET turn-on, the charge of C is limited to forward voltage drop of D. By consequent, the JFET in On-state has a better On-resistance. R_p is of high value (several kΩ) and limits the gate current under punch-through condition only when the JFET is an Off-state.
So the advantage of this topology is to give the possibility to tune the blocking voltage below $V_{br,gs}$ since the protection against the punch-through in static mode is insured. In other words, this topology can compensate V_{T0} variation from device to device. However, drain-to-gate interaction effects (both punch-through and short-circuit of the JFET leg) are not minimized because during each switching the gate current can flow through the capacitor C. Furthermore, it should be noticed that the ambient temperature plays an important role to design this specific SiC JFET gate driver circuit.

- The last one (Fig. 15-c). proposed in [7] is a trade-off between the two topologies presented before (topologies *a* and *b* in Fig. 15). Unfortunately, this structure does not allow to combine the advantages of *a* and *b*. Indeed, there is no component between C_G and the JFET Gate to limit the gate current due to the punch-through effect when the blocking voltage is under $V_{br,gs}$. In addition, R_p is not useful when the blocking voltage is between V_{T0} and $V_{br,gs}$.

4 Prototype

A prototype (Fig. 16) is built using a hermetic Si3N4 module packaged by SEMELAB (Fig. 17) housing six SiC JFET from SiCED and a ceramic capacitor form AVX, assembled on a high temperature printed circuit board. Fig. 16 represents the module and the dc-link capacitor. The dc-link capacitor is implemented as close as possible to the module in order to reduce the parasitic inductor. Thus the over-voltage across the JFET during switching is decreased. The inverter is piloted using six specific gate drivers.

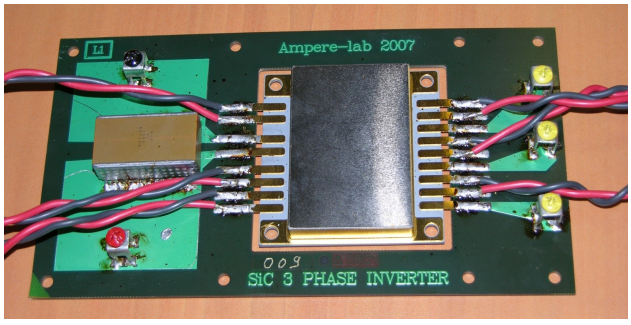

Fig. 16: Power Inverter Module

Characteristics of the Power Inverter Module exhibited in Fig. 16 are summarized below,

- 15A 1200V SiC JFET are used, the junction temperature can reach 300°C without degradation;
- The Si3N4 substrate can withstand temperature of 600°C;
- Bonding are made with Al/Ag 125µm and the temperature limit is 400°C;
- Encapsulating GEL limits is 260 °C with possible peak of 300°C;
- Die brazing on substrate is Au/Ge 370°C;

- Hermetic package is used in order to reduce the corrosion.

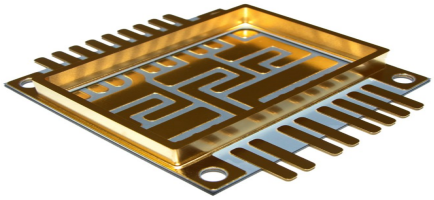

Fig. 17: Power Inverter Module packaged by SEMELAB

The driver schematic is presented in Fig. 18. The purpose of the driver is to convert a control signal sent by the Microprocessor to a Power signal that set the output state of the power switch. As mentioned previously, the JFET is turn on by applying a negative voltage across the gate and the source. Therefore a specific driver has been designed for SiC JFETs. The output stage is a classical push-pull stage with a current capability of around 2A. The insulation between the control side and power side is achieved with opto-coupler. As explained in the previous section, a gate protection may be implemented in order to reduce the interaction between the power side (Drain) and the control side (Gate). The dv/dt immunity is greater than 35 kV/µs.
The driver provides also means of protection such as DESAT (over current protection) and Under Voltage Lockout (UVLO).

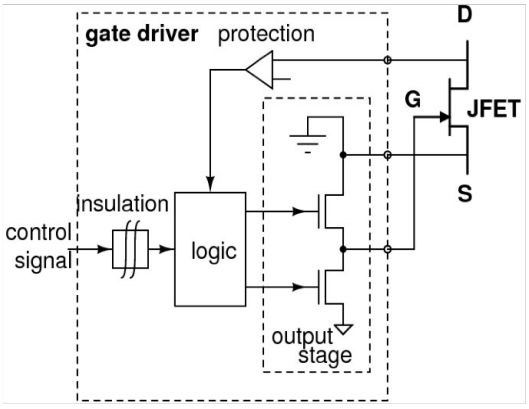

Fig. 18: Driver Functional Description

At the time of testing the drivers low temperature versions were used and therefore drivers were remote from the inverter during temperature testing in the oven. That is why the cable length between the inverter and gate drivers are so long. At the time of writing, driver using SOI MOSFET technologies (Fig. 19) has been built, tested and validated up to 200°C and 540V. Moreover, the parasitic inductance between the driver and the inverter has been reduced and better switching performance has been observed. However, the whole Power Inverter Module is under testing and no results are shown.

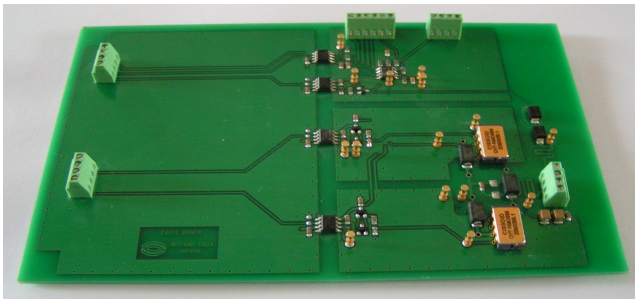

Fig. 19: Driver using SOI MOSFET technology from CISSOID

5- Experimental Characterizations at the Inverter Level.

The inverter is tested at power levels of 540 V and 8 A, and heated up to 200 °C. Fig. 20 and Fig. 21 depict the turn-on and turn-off switching characterization. The green, red, purple and dark blue curves represent the drain-to-source voltage, the gate current, the gate voltage and the drain current respectively.
The switching time at turn-on is 200 ns (47 Ω gate resistor) and 300 ns at turn off. The switching losses are equals to 498 µJ at turn on and 251 µJ at turn-off. As expected, the highest losses occur at turn-on when the opposite JFET produces a peak current caused by a recovery mechanism, linked to the value of the current and the temperature.
For both turn-on and off, we can notice the 'Miller Plateau' (gate to source voltage constant) where the gate to drain capacitance is discharged/charged by the gate driver. The driver's gate energy has been measured. At turn-on, the energy needed to close the JFET is equal to 0.9 µJ whereas at turn-off the driver provides 0.5 µJ of energy to bloc the JFET.

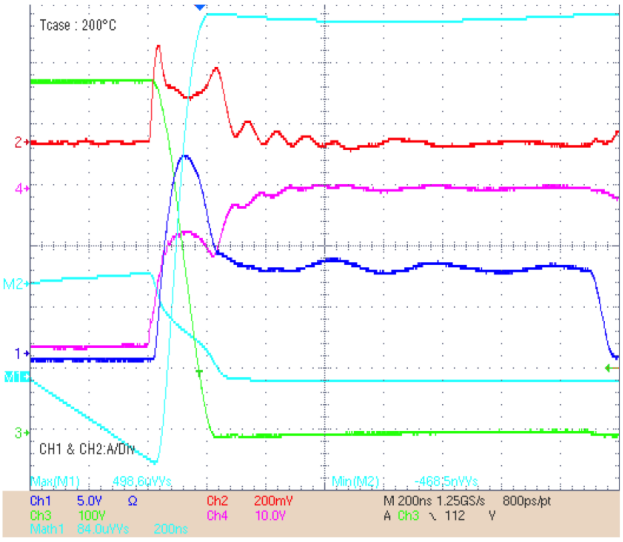

Fig. 20: Turn-on measurements during an inverter operation at 540V, 15A and 200°C

The output voltage and current of a phase leg is depicted in Fig. 22. The red curve represents the phase voltage and the yellow curve the phase current. The switching frequency is 20KHz.

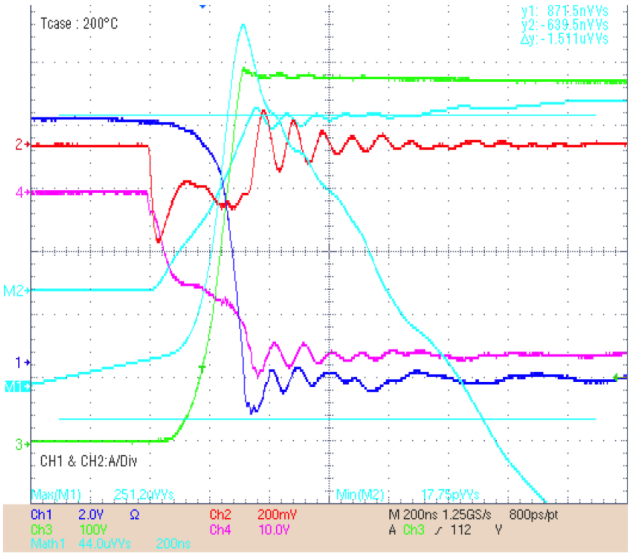

Fig. 21: Turn-off measurements during an inverter operation at 540V, 15A and 200°C

6 Conclusion

Based on SiC-JFETs from SiCED/INFINEON inverter modules were fabricated on Si_3N_4 substrates. Demonstrators were achieved in the framework of the SEFORA project. Each modules includes 6 bare dies of SiC-JFETs. These modules were fabricated on 2.4 x 2.4 dies. The possible degradation of the JFET internal diodes because of the diode-less operation of the inverter was studied. It has been shown that no significant degradation may be observed. The obtained efficiency is about 94% at 200 °C. The new generation of JFETs having an area of 4.16 x 4.16 mm² were characterized. They yield to a reduction of the on-losses with a ratio of 3, and consequently the efficiency may reach 97%. The operation was shown at the device level, the interaction with respect to gate drivers.

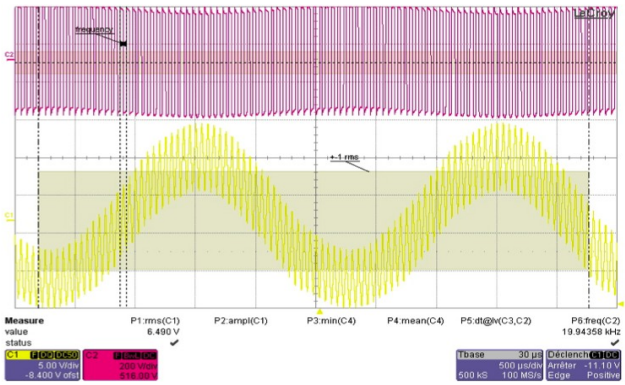

Fig. 22: line current and output voltage measurements during an inverter operation at 540V, 15A and 200°C

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